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(54) **TEST STRUCTURE AND METHOD FOR DETERMINING OVERLAY ACCURACY IN SEMICONDUCTOR DEVICES USING RESISTANCE MEASUREMENT**

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(57) **ABSTRACT**

Provided is a test pattern structure for determining overlay accuracy in a semiconductor device. The test pattern structure includes one or more resistor structures formed by patterning a lower silicon layer. Each includes a zigzag portion with leads at different spatial locations. An upper pattern is formed and includes at least one pattern feature formed over the resistor or resistors. The portions of the resistor or resistors not covered by the upper pattern feature will become silicided during a subsequent silicidation process. Resistance is measured to determine overlay accuracy as the resistor structures are configured such that the resistance of the resistor structure is determined by the degree of silicidation of the resistor structure which is determined by the overlay accuracy between the upper and lower patterns.

20 Claims, 5 Drawing Sheets
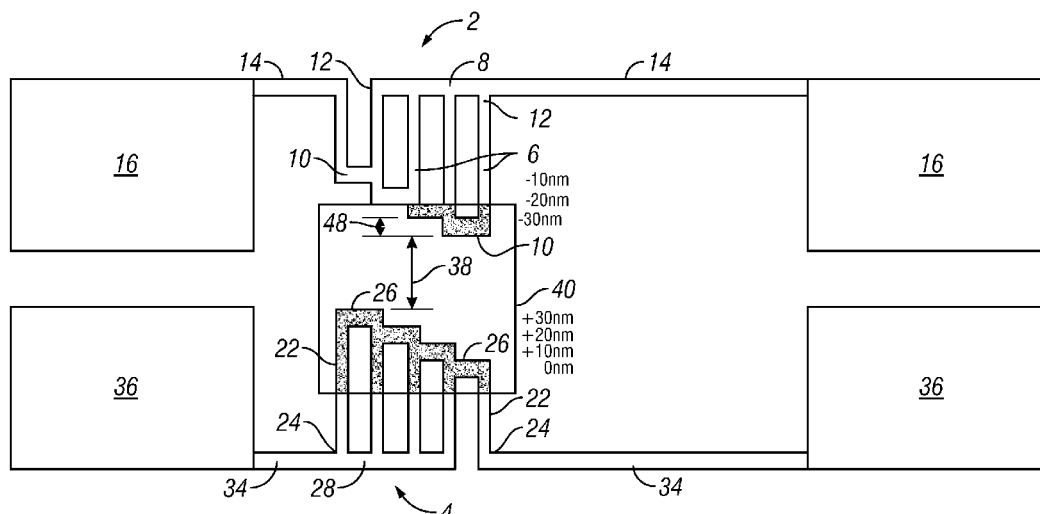
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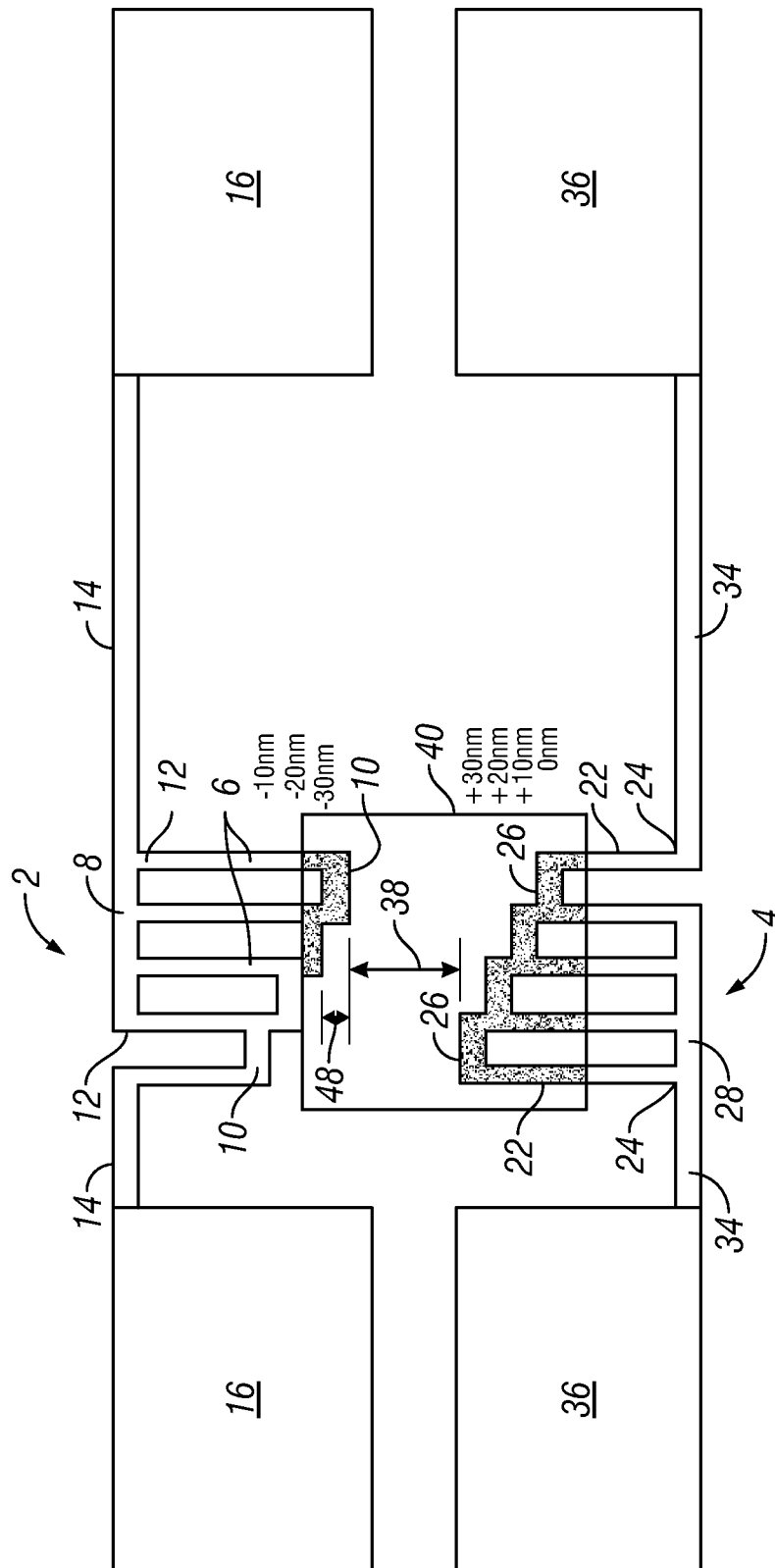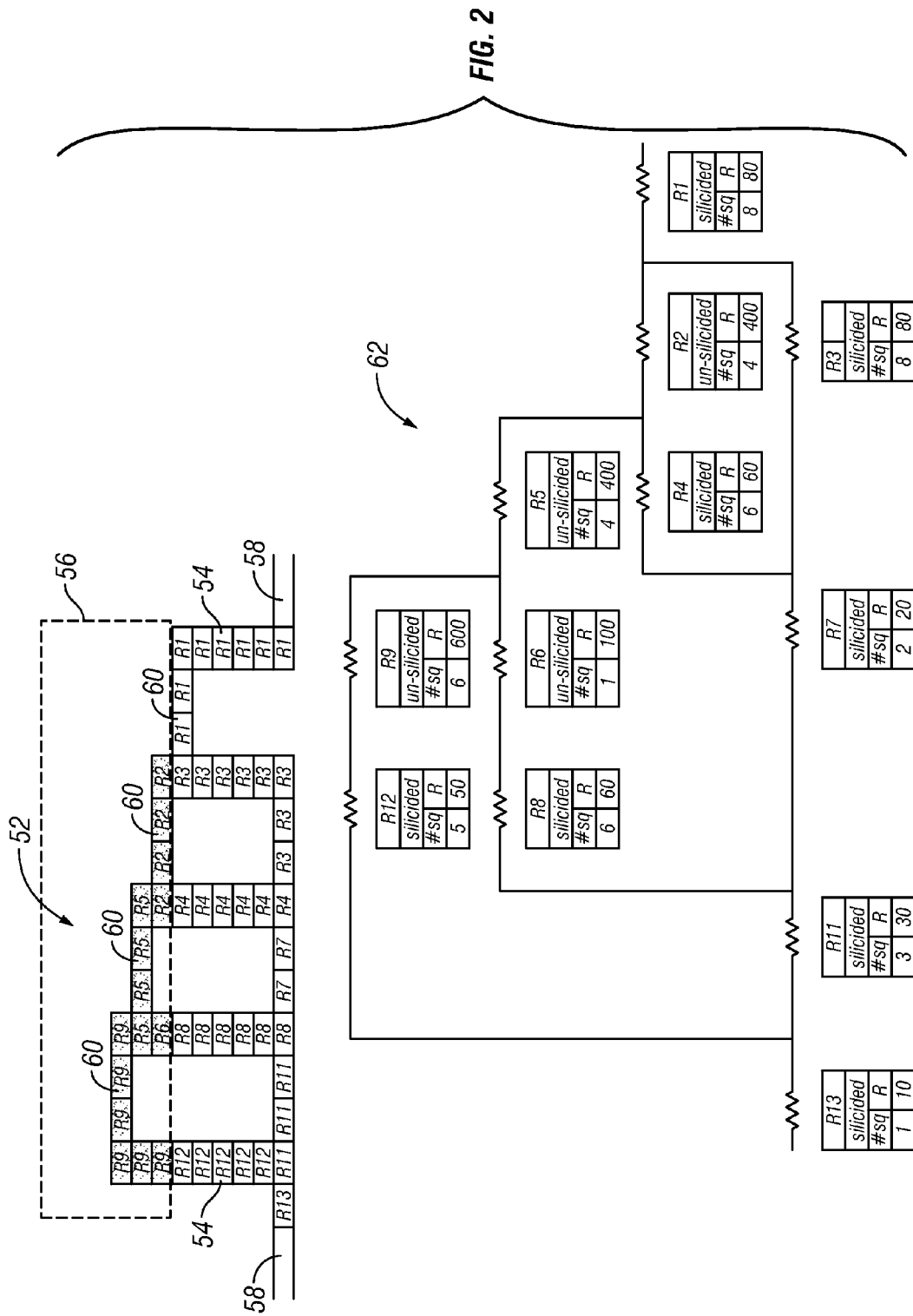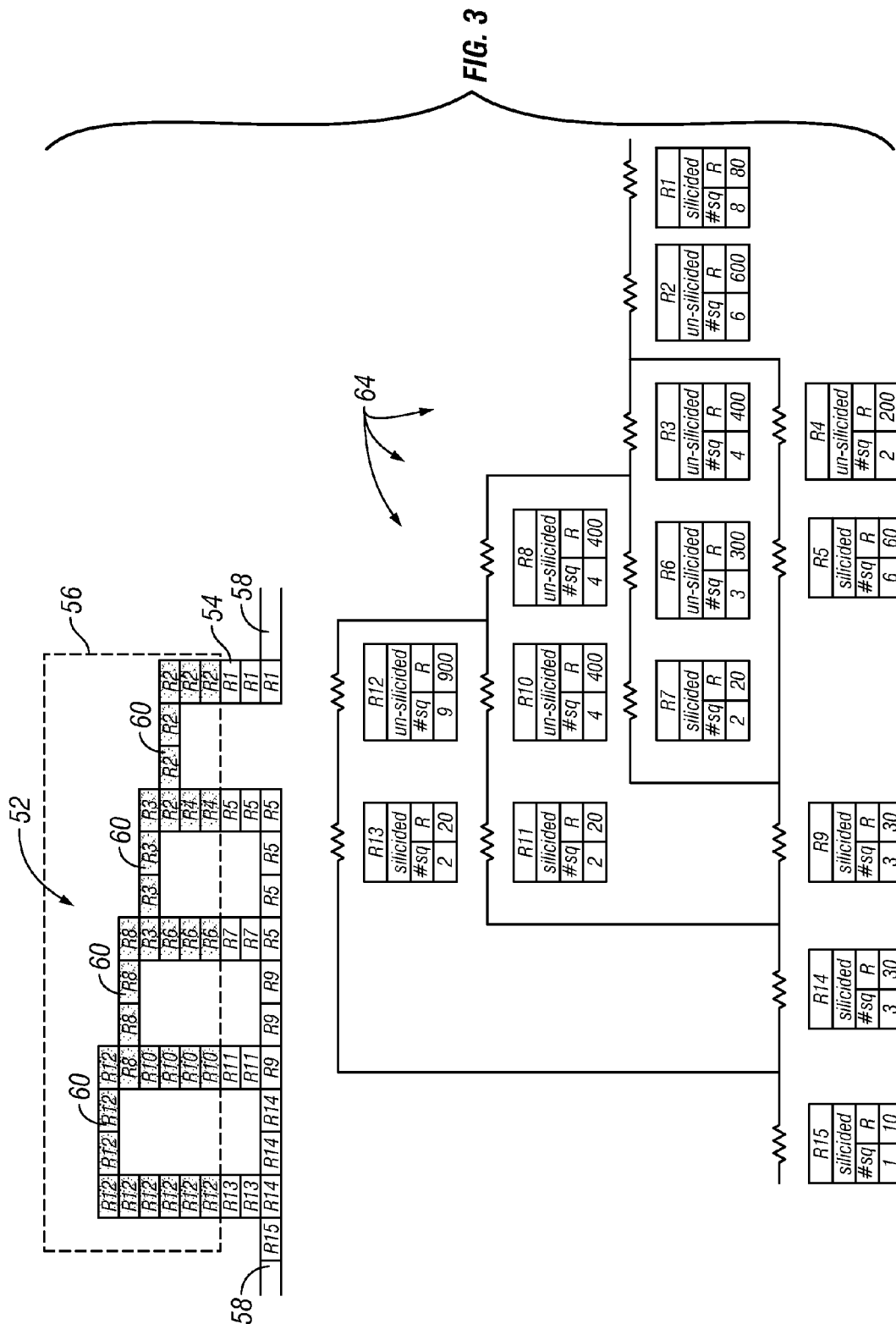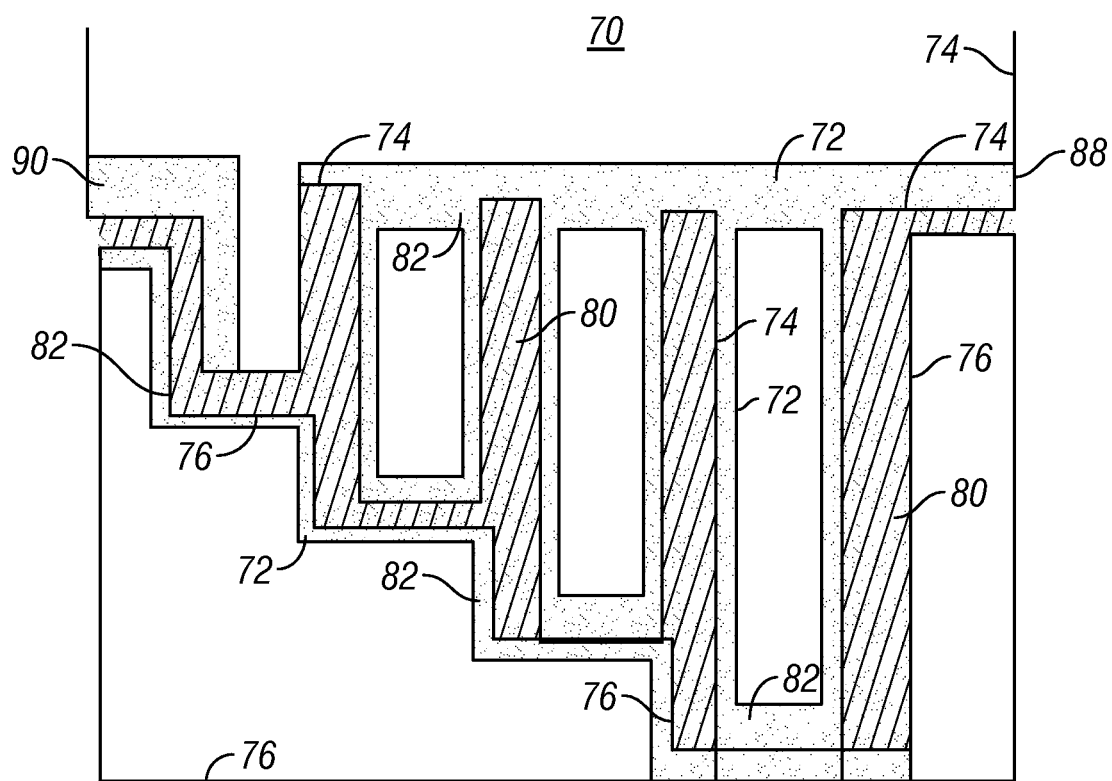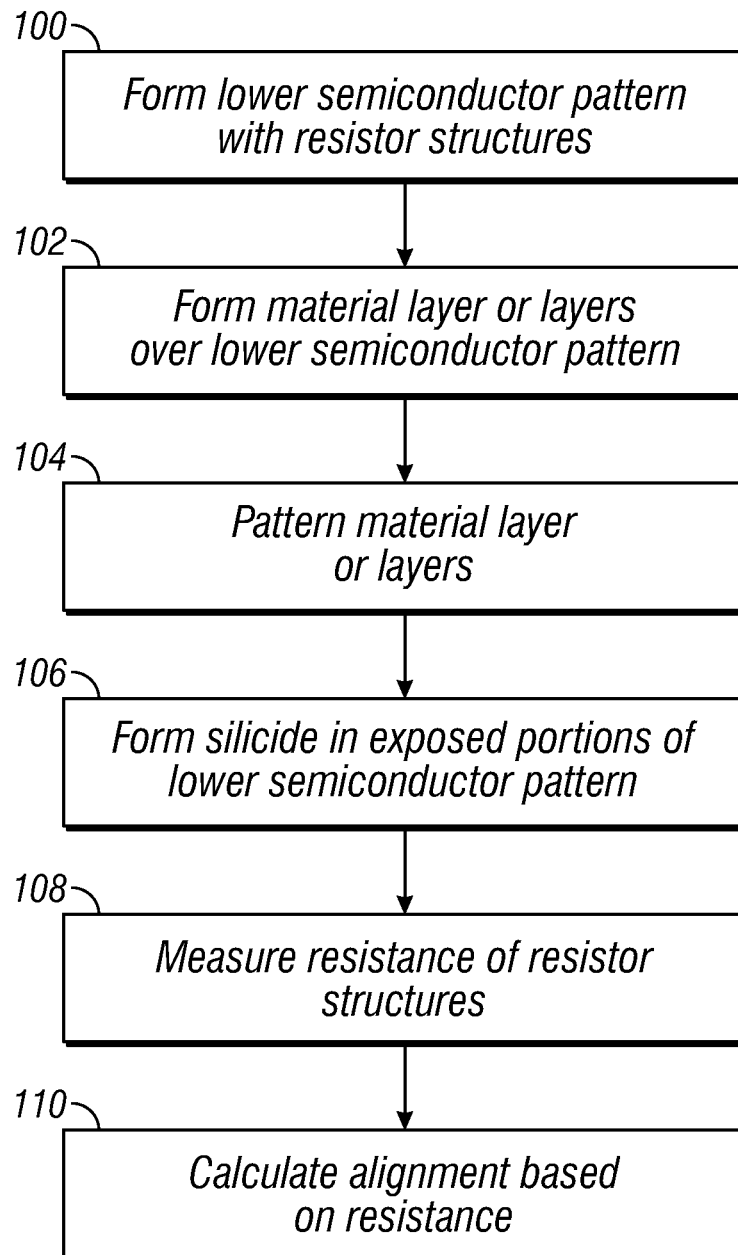
-10nm
-20nm
-30nm

+30nm
+20nm
+10nm
0nm

FIG. 1

FIG. 2

FIG. 3

FIG. 4

100 ⌐

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Form lower semiconductor pattern
with resistor structures
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102 ⌐

```
Form material layer or layers
over lower semiconductor pattern
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104 ⌐

```
Pattern material layer
or layers
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106 ⌐

```
Form silicide in exposed portions of
lower semiconductor pattern
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108 ⌐

```
Measure resistance of resistor
structures
```

110 ⌐

```
Calculate alignment based
on resistance
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FIG. 5

TEST STRUCTURE AND METHOD FOR DETERMINING OVERLAY ACCURACY IN SEMICONDUCTOR DEVICES USING RESISTANCE MEASUREMENT

TECHNICAL FIELD

The disclosure relates to semiconductor devices, and more particularly to electrical test structures and methods for determining overlay accuracy or misalignment between patterns of different semiconductor device layers using resistance measurements.

BACKGROUND

As semiconductor devices continue to advance and become more highly integrated and as the device features become increasingly miniaturized, the alignment between one device level and another device level increases in criticality. The patterns that combine to form integrated circuit or other semiconductor devices must be accurately and precisely aligned to one another, i.e. each pattern must be properly overlaid with respect to existing patterns. Embedded flash products represent one particular example of a product that requires stringent overlay control at various levels such as the floating gate level, in order to minimize program state leakage. While such embedded flash products may be particularly sensitive to overlay accuracy, it is important to accurately align every device level of every semiconductor device with each of the previously formed device levels, so that each device level functions as intended, in conjunction with each subjacent layer.

In conventional processing, overlay accuracy is typically measured using optical metrology tools. Such optical measurements are time consuming and subject to inaccuracies due to optical metrology limitations. Since the time-consuming optical measurements are typically required to be fed back to the exposure tool, only a limited number of optical measurements are made to determine overlay accuracy, in order to minimize time delays.

It would therefore be desirable to measure the overlay of respective layers using a technique that does not include the shortcomings and limitations of optical overlay measurement and which accurately and quickly provides overlay measurements of the substrate being processed.

BRIEF DESCRIPTION OF THE DRAWING

The present disclosure is best understood from the following detailed description when read in conjunction with the accompanying drawing. It is emphasized that, according to common practice, the various features of the drawing are not necessarily to scale. On the contrary, the dimensions of the various features may be arbitrarily expanded or reduced for clarity. Like numerals denote like features throughout the specification and drawing.

FIG. 1 is a plan view of a set of test resistor structures overlaid with a further pattern according to an aspect of the disclosure;

FIG. 2 is a plan view showing an exemplary underlying resistor structure with a portion silicided, and an associated resistance circuit diagram;

FIG. 3 is a plan view showing the same exemplary underlying resistor structure as in FIG. 2, but having a lesser portion silicided, and the associated resistance circuit diagram;

FIG. 4 is a plan view showing a resistor structure, two overlying patterns and with exposed portions of the resistor structure being silicided; and

FIG. 5 is a flow chart illustrating an exemplary method of the disclosure.

DETAILED DESCRIPTION

The disclosure provides a resistor structure formed of a semiconductor material in a lower layer of a semiconductor device. The resistor structure is advantageously disposed in a test portion of a substrate as part of a lower pattern that also includes active semiconductor device features in active device portions. One exemplary resistor structure includes a zigzag structure which includes orthogonal features and can alternatively be described as a step structure or a structure of interconnected fingers. The resistor structure may include a series of parallel leads having different lengths and coupled by transverse leads that extend orthogonally with respect to the parallel leads. The resistor structure may advantageously be paired with a second resistor structure that faces the first resistor structure. The second resistor structure also has parallel leads that may be parallel to the series of parallel leads of the first resistor structure and the second resistor structure may be the mirror image of the first resistor structure in one exemplary embodiment. The second resistor structure is also formed of the lower layer of semiconductor material. Each resistor structure includes transverse leads spaced different distances from the other of the resistor structures.

An upper pattern in a further material layer or layers is formed overlaying the lower pattern and includes a structure or structures over the resistor structures such that the degree of overlay accuracy can be assessed by the number of transverse leads covered by the structure or structures of the overlying pattern. A silicidation process forms a silicide only on exposed portions of the resistor structures, i.e., portions not covered by the upper pattern. Electrical measurements are made from opposed ends of the resistor structures. In particular, the resistance of each resistor structure is measured. The resistance is dependent upon the amount of the resistor structure that has been silicided. In this manner, the measured electrical resistance measurements are indicative of the degree of overlay accuracy.

In other exemplary embodiments, only one resistor structure may be used and in another exemplary embodiment a set of four resistor structures may be used to determine overlay accuracy between the lower pattern and the upper pattern in more than one direction such as the x- and y-directions. The resistor structures or sets of resistor structures may be placed at multiple locations on a substrate being processed. Each of the previous exemplary embodiments can be used to show the accuracy of overlay between the lower pattern and the upper pattern.

According to another exemplary embodiment, a zigzag or step-like structure of a resistor formed as part of a pattern of a lower semiconductor layer is used to determine overlay accuracy between two other patterns formed over the lower semiconductor layer pattern.

FIG. 1 is a plan view showing a set of complementary resistor structures formed of semiconductor materials in a lower semiconductor layer. First resistor structure 2 and second resistor structure 4 are formed of a material capable of having a silicide formed thereon, i.e. silicon. According to one exemplary embodiment, first resistor structure 2 and second resistor structure 4 may represent the active area pattern of a semiconductor device, i.e., the surface of a silicon substrate bounded by a dielectric such as a field oxide and formed

during an active area or "oxide definition" patterning operation. According to other exemplary embodiments, first resistor structure 2 and second resistor structure 4 may be a polysilicon layer such as the layer used for a floating gate electrode in a floating gate flash product. Conventional or other methods may be used to pattern first resistor structure 2 and second resistor structure 4. First resistor structure 2 and second resistor structure 4 represent a part of a lower pattern formed in a lower semiconductor material. First resistor structure 2 and second resistor structure 4 are formed in a test portion on a semiconductor substrate and other portions of the lower pattern formed of the lower semiconductor material include active device structures formed in active device portions. First resistor structure 2 and second resistor structure 4 may be any suitable silicon material and are part of a pattern that includes active features formed in active portions of a semiconductor device and to which superjacent pattern features must be aligned.

First resistor structure 2 includes a series of parallel leads 6 with upper ends 12 coupled by base lead 8 in the illustrated orientation. Opposed lower ends of parallel leads 6 are coupled by transverse leads 10 which extend orthogonally from parallel leads 6. Transverse leads 10 are spaced different distances from second resistor structure 4 and couple one parallel lead 6 to an adjacent parallel lead 6. Parallel leads 6 include increasingly longer lengths going from left to right in the illustrated orientation, i.e., along one direction orthogonal to direction 38 between first resistor structure 2 and second resistor structure 4. Distance 48 between the terminal edges of adjacent transverse leads 10 may vary and may be about 10 nm in one exemplary embodiment but will vary in other exemplary embodiments. The lower portion of first resistor structure 2 as illustrated in FIG. 1 can be described as a step-structure or as a zigzag structure, but it should be understood that the illustrated embodiment is intended to be exemplary only and the number of parallel leads 6 may vary in other exemplary embodiments as will the number of transverse leads 10. The relative size and configuration of transverse leads 10 and parallel lead 6 is also exemplary only.

Second resistor structure 4 is essentially the mirror image of first resistor structure 2 in the exemplary illustrated embodiment, and includes parallel leads 22 and transverse leads 26, parallel leads 22 joined together by base lead 28 at ends 24. Parallel leads 22 include increasingly longer lengths going from right to left in the illustrated orientation.

The illustrated representation in which first resistor structure 2 and second resistor structure 4 are of the same approximate dimension and are mirror images of one another, represents an advantageous exemplary embodiment but in other exemplary embodiments, first resistor structure 2 and second resistor structure 4 may be dissimilar and include different sizes and configurations.

First resistor structure 2 is coupled to opposed contact pads 16 by way of metal leads 14. The resistance of first resistor structure 2 can be measured electrically by contacting each contact pad 16 which may be formed of metal according to various exemplary embodiments. Similarly, second resistor structure 4 is coupled to opposed contact pads 36 by way of respective metal leads 34 and the resistance of second resistor structure 4 can be measured electrically by contacting each contact pad 36 which may be formed of metal. Conventional or other techniques may be used to measure resistance.

An upper pattern is formed over the lower pattern of semiconductor material and includes upper pattern feature 40 formed over first resistor structure 2 and second resistor structure 4. Upper pattern feature 40 may represent a void in an upper material layer or layers or it may represent a discrete

portion of an upper material layer or layers, and the disclosure provides for determining the overlay accuracy between upper pattern feature 40 and first and second resistor structures 2 and 4 which represents the overlay accuracy between the upper and lower patterns.

The illustrated structure showing first resistor structure 2, second resistor structure 4 and upper pattern feature 40 may be formed in a test portion of an integrated circuit chip or in a scribe line on a semiconductor substrate and this arrangement may be formed on multiple locations on the semiconductor substrate so that the overlay accuracy between the upper and lower patterns can be assessed throughout the entire semiconductor substrate. Upper pattern feature 40 represents a pattern feature formed in a test portion and is part of a device pattern formed in active device portions of the semiconductor device which act in conjunction with and are aligned with the lower semiconductor pattern. In one exemplary embodiment, the lower semiconductor pattern may be the active area definition of a semiconductor device and the upper pattern including upper pattern feature 40 may be the floating gate of a flash product and according to another exemplary embodiment, the lower semiconductor pattern may be the active area definition of a semiconductor device and the upper pattern including upper pattern feature 40 may be a polysilicon layer, an RPO layer or any other semiconductor or conductive layer. According to yet another exemplary embodiment, the lower semiconductor pattern including first resistor structure 2 and second resistor structure 4 may be the floating gate pattern and the upper pattern including upper pattern feature 40 may be a polysilicon layer used as an upper gate layer in a floating gate transistor in an embedded flash product.

Still referring to FIG. 1, the degree of overlay accuracy between upper pattern feature 40 and first and second resistor structures 2 and 4 in the y-direction is indicated by the number of transverse leads 10 and 26 that are covered by upper pattern feature 40. For example, if alignment in the y-direction was perfect, equal numbers of transverse leads would be covered by upper pattern feature 40 for each of first resistor structure 2 and second resistor structure 4, and first resistor structure 2 and second resistor structure 4 would have the same resistance after a silicidation operation.

According to one advantageous embodiment, the structure shown in FIG. 1 is formed in close proximity to another example of the structure shown in FIG. 1, but rotated 90 degrees so that overlay accuracy in both the x- and y-directions can be assessed.

Still referring to FIG. 1, the upper pattern including upper pattern feature 40 may be formed of a composite material layer including an upper layer being one of the aforementioned polysilicon layers and underlying interlevel dielectric layer. According to this exemplary embodiment, the polysilicon portion of the upper pattern is electrically isolated from the semiconductor material of first and second resistor structures 2 and 4. After the exemplary pattern is formed as shown in FIG. 1, silicidation takes place. Conventional or other silicidation techniques may be used, such as forming a metal layer over the entire semiconductor substrate being processed then heating to form a silicide on exposed surfaces such as the exposed surfaces of first resistor structure 2 and second resistor structure 4 not covered by upper pattern feature 40. The extent of silicidation of first resistor structure 2 and second resistor structure 4 will determine its resistance.

The resistance of first resistor structure 2 and second resistor structure 4 is extremely sensitive to the amount of the structure which has undergone silicidation. According to one exemplary embodiment, the sheet resistance of unsilicided polysilicon may be about 200 ohms/sq. whereas the sheet

resistance of polysilicide may be about 4 ohms/sq. Such is exemplary only but this is indicative of the sensitivity of the resistor structures to the amount of the resistor structure that has undergone silicidation.

FIGS. 2 and 3 each show a top view of a partially silicided resistor structure and the associated resistance circuit diagram. In this exemplary embodiment, resistance for unsilicided silicon is 100 ohms/sq. and resistance for silicided silicon is 10 ohms/sq. The same resistor structure 52 is shown in each of FIGS. 2 and 3 but the relative amount of silicided portion 54 and unsilicided portion 56 is different. In resistor structure 52 illustrated in FIG. 2, silicided portion 54 represents a greater portion of resistor structure 52 than in the resistor structure 52 shown in FIG. 3. In particular, more transverse leads 60 are not silicided in the resistor structure 52 of FIG. 3. As such, the associated resistance circuit diagrams 62 and 64 show that the resistance for the resistor structure 52 shown in FIG. 3 is greater than the resistance for the resistor structure 52 shown in FIG. 2. The resistance is the resistance as measured across resistor structure 52 by contacting conductive features coupled to opposed conductive leads 58 using conventional known methods.

FIG. 4 illustrates another exemplary embodiment of the disclosure. Resistor structure 72 represents part of a lower pattern formed of semiconductor material and resistor structure 72 may be formed in or on semiconductor substrate 70, similar to the lower semiconductor pattern as described in conjunction with FIG. 1. Resistor structure 72 is formed of a material such as silicon that can undergo silicidation on its exposed surfaces. Resistor structure 72 represents a structure of a lower pattern formed in a test portion of a substrate, other portions of which are formed in active portions of the semiconductor device. Resistance of resistor structure 72 can be measured across opposed ends 88, 90 using various known means and the resistance of resistor structure 72 will depend upon the amount of resistor structure 72 which has undergone silicidation because the silicidation of a silicon surface reduces resistance, and due to the sensitivity of the resistance upon the amount of resistor structure 72 that has been silicided.

Upper patterns 74, 76 are each formed over resistor structure 72 and are each part of a device level that includes structures formed in active portions of the integrated circuit or other semiconductor device die. Each of upper patterns 74 and 76 may be formed of one or more material layers used in the formation of semiconductor devices. Upper pattern 74 may be formed before and beneath upper pattern 76, or vice versa. After the formation of upper patterns 74 and 76, resistor structure 72 includes two different portions: portions 82 that are covered by one or both of upper patterns 74, 76 and exposed portions 80 that are not covered by either of upper patterns 74 or 76. After a conventional silicidation process is carried out, only exposed portions 80 of resistor structure 72 are silicided. The relative amounts of covered portions 82 and exposed portions 80 will determine the resistance of resistor structure 72 as measured across ends 88 and 90.

The overlay accuracy between upper patterns 74 and 76 can be assessed by the resistance across resistor structure 72. According to one exemplary embodiment, accurate alignment between upper patterns 74 and 76 would include a gap between upper patterns 74 and 76 over resistor structure 72 such that a continuous path of silicided material is available from one end 88 to the opposed end 90 thereby producing a low resistance. The number of voids in an otherwise continuous path of silicide material from end 88 to end 90, will significantly impact resistance and is indicative of alignment between upper patterns 74 and 76. This is intended to be

exemplary only and in other exemplary embodiments, resistor structure 72 and upper patterns 74 and 76 may be differently configured provided resistor structure 72 includes segments that will be exposed or covered depending on the positioning of upper patterns 74 and 76, i.e. depending on the alignment between upper patterns 74 and 76 and the alignment between upper patterns 74 and 76 and resistor structure 72. A subsequent silicidation process produces silicided and non-silicided sections such that the resistance across resistor structure 72 is indicative of which segments are silicided and not silicided, which, in turn, is indicative of the alignment or overlay of upper pattern 74 with respect to upper pattern 76.

FIG. 5 shows a flow chart of an exemplary method of the invention. At step 100, a lower semiconductor pattern is formed of semiconductor material in active portions of the semiconductor device and also in a test portion which includes a resistor structure or structures. There may be one resistor structure, a pair of resistor structures, or multiple pairs of resistor structures oriented to assess alignment in multiple directions. At step 102, a material layer or layers is formed over the lower semiconductor pattern and will advantageously include a lower dielectric layer over the lower semiconductor pattern. At step 104, the material layer or layers is patterned to form active device features in active device portions and also a pattern feature overlying the resistor structure or structures. At step 106, a silicide is formed in exposed portions of the lower semiconductor pattern including the resistor structures and at step 108, resistance of the resistor structure or structures is measured.

At step 110, alignment accuracy is assessed. As shown in FIGS. 1-3, the resistance of the resistor structure is dependent upon the amount of that resistor structure that has undergone silicidation and the amount of the resistor structure that has undergone silicidation is dependent upon the alignment of the overlying pattern of the material layer or layers. Because of the significant difference between sheet resistance in silicided and unsilicided portions, the overall resistance is very sensitive to the amount of the resistor structure or structures that has been silicided. When two resistor structures are presented in a pair such as shown in FIG. 1, the resistance difference between first resistor structure 2 and second resistor structure 4 is indicative of the relative position of upper pattern feature 40 along the y-direction in the illustrated orientation. According to one exemplary embodiment, perfectly accurate overlay, i.e. perfect alignment, will result in first resistor structure 2 and second resistor structure 4 having the same resistance. According to the embodiment in which a structure similar to the structure shown in FIG. 1 is formed in close proximity to the structure shown in FIG. 1 and rotated 90 degrees, multiple resistance measurements can be used to assess the alignment accuracy in both the x- and y-directions.

For each particular resistor structure or pairs of resistor structures, a correlation can be generated between the measured resistance and the number of segments such as transverse leads 10 and 26 (see FIG. 1) that have undergone silicidation based on the layout of the resistor structures. The number of such transverse leads that have undergone silicidation is directly dependent upon the location and therefore overlay between the upper pattern feature 40 and the lower resistor structures. The correlations may be based upon the resistor circuit diagrams such as shown in FIGS. 2 and 3 or other mathematical models. The measurements carried out at step 108 may be automatically carried out and may be carried out at multiple locations across a semiconductor substrate.

According to one aspect, provided is a test pattern structure in a semiconductor device for determining pattern overlay accuracy. The test pattern includes a lower semiconductor

pattern of the semiconductor material bounded by a dielectric. The semiconductor pattern includes a first resistor structure and a second resistor structure. Each of the resistor structures includes a zigzag portion including transverse leads disposed orthogonal to a direction from the first resistor to the second resistor and each of the first resistor structure and second resistor structure include the transverse leads spaced at different distances from the other of the resistor structures.

According to another aspect, provided is a method for determining overlay accuracy in a semiconductor device. The method comprises forming a lower semiconductor pattern of a semiconductor material bounded by a dielectric, the lower semiconductor pattern including a first resistor structure and a second resistor structure, forming an overlying pattern in a material layer or layers over the semiconductor pattern, siliciding exposed portions of the first resistor structure and second resistor structure, not covered by the overlaying pattern, measuring a first resistance of the first resistor structure and measuring a second resistance of the second resistor structure, and calculating overlay accuracy between the overlying pattern and the lower semiconductor pattern based on the first resistance and second resistance.

According to another aspect, the disclosure provides a method for determining overlay accuracy in a semiconductor device. The method comprises forming a lower semiconductor pattern of a semiconductor material bounded by a dielectric, the lower semiconductor pattern including at least a resistor structure, forming a first overlying pattern in a first material layer or layers over the semiconductor pattern, forming a second overlying pattern in the second material layer or layers over the semiconductor pattern and siliciding exposed portions of the lower semiconductor pattern not covered by the first overlying pattern or the second overlying pattern. The method further includes measuring resistance of the resistor structure and calculating alignment accuracy between the first overlying pattern and the second overlying pattern based on resistance.

The preceding merely illustrates the principles of the disclosure. It will thus be appreciated that those skilled in the art will be able to devise various arrangements which, although not explicitly described or shown herein, embody the principles of the disclosure and are included within its spirit and scope. Furthermore, all examples and conditional language recited herein are principally intended expressly to be only for pedagogical purposes and to aid in understanding the principles of the disclosure and the concepts contributed by the inventors to furthering the art, and are to be construed as being without limitation to such specifically recited examples and conditions. Moreover, all statements herein reciting principles, aspects, and embodiments of the disclosure, as well as specific examples thereof, are intended to encompass both structural and functional equivalents thereof. Additionally, it is intended that such equivalents include both currently known equivalents and equivalents developed in the future, i.e., any elements developed that perform the same function, regardless of structure.

This description of the exemplary embodiments is intended to be read in connection with the figures of the accompanying drawing, which are to be considered part of the entire written description. In the description, relative terms such as "lower," "upper," "horizontal," "vertical," "above," "below," "up," "down," "top" and "bottom" as well as derivatives thereof (e.g., "horizontally," "downwardly," "upwardly," etc.) should be construed to refer to the orientation as then described or as shown in the drawing under discussion. These relative terms are for convenience of description and do not require that the apparatus be con-

structed or operated in a particular orientation. Terms concerning attachments, coupling and the like, such as "connected" and "interconnected," refer to a relationship wherein structures are secured or attached to one another either directly or indirectly through intervening structures, as well as both movable or rigid attachments or relationships, unless expressly described otherwise.

Although the disclosure has been described in terms of exemplary embodiments, it is not limited thereto. Rather, the appended claims should be construed broadly, to include other variants and embodiments of the disclosure, which may be made by those skilled in the art without departing from the scope and range of equivalents of the disclosure.

What is claimed is:

1. A method for determining overlay accuracy in a semiconductor device, said method comprising:

   forming a lower semiconductor pattern of a semiconductor material bounded laterally by a dielectric, said lower semiconductor pattern including a first resistor structure and a separate second resistor structure formed of the same material layer and physically separated from said first resistor structure;

   forming an overlying pattern in a further material layer or layers, disposed over said lower semiconductor pattern;

   siliciding exposed portions of said first resistor structure and said second resistor structure not covered by said overlying pattern;

   measuring a first resistance of said first resistor structure and measuring a second resistance of said second resistor structure; and

   calculating overlay accuracy between said overlying pattern and said lower semiconductor pattern based on said first resistance and said second resistance.

2. The method as in claim 1, wherein said forming a lower semiconductor pattern includes forming said first resistor structure and said second resistor structure in at least one test portion and forming active device structures in active device portions of a semiconductor device, on a semiconductor substrate, and

   said forming an overlying pattern includes forming portions in said at least one test portion and in said active device portions.

3. The method as in claim 1, wherein said forming an overlying pattern comprises depositing said further material layer or layers, forming a photolithographic pattern over said further material layer or layers, then etching, said etching exposing said exposed portions of said first resistor structure and said second resistor structure, and wherein said further material layer or layers blocks silicidation of covered portions of said lower semiconductor pattern including said first resistor structure and said second resistor structure.

4. The method as in claim 1, wherein said lower semiconductor pattern comprises an active area pattern, said semiconductor material comprising a silicon surface of a semiconductor substrate and said dielectric comprises a field oxide.

5. The method as in claim 1, wherein said lower semiconductor pattern comprises a polysilicon pattern.

6. The method as in claim 1, wherein said lower semiconductor pattern includes each of said first and second resistor structures having a plurality of parallel leads having different lengths and coupled to one another by orthogonal leads.

7. The method as in claim 6, wherein said parallel leads of said first resistor structure are parallel to said parallel leads of said second resistor structure, longer ones of said parallel leads of said first resistor structure extend closer to said second resistor structure than shorter ones of said parallel leads of said first resistor structure, and said first resistor structure

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includes said parallel leads having respective lengths that increase progressively along a first orthogonal direction and said second resistor structure includes said parallel leads having respective lengths that decrease progressively along said first orthogonal direction.

8. The method as in claim 6, wherein, for each of said first and second resistor structures, each of said parallel leads includes one end that terminates at the same perpendicular location and an opposed end joined to an adjacent one of said parallel leads, by one said orthogonal lead, said opposed ends and said orthogonal leads forming a step-like structure in each of said first and second resistor structures.

9. A method for determining overlay accuracy in a semiconductor device, said method comprising:

forming a lower semiconductor pattern of a semiconductor material bounded laterally by a dielectric, said lower semiconductor pattern including a first resistor structure and a separate second resistor structure formed of the same material layer;

forming an overlying pattern in a further material layer or layers, disposed over said lower semiconductor pattern;

siliciding exposed portions of said first resistor structure and said second resistor structure not covered by said overlying pattern;

measuring a first resistance of said first resistor structure and measuring a second resistance of said second resistor structure; and

calculating overlay accuracy between said overlying pattern and said lower semiconductor pattern based on said first resistance and said second resistance,

wherein each of said first resistor structure and said second resistor structure comprises a zigzag portion including transverse leads disposed orthogonal to a direction from said first resistor structure to said second resistor structure, said transverse leads including first transverse leads of said first resistor structure spaced at different distances from said second resistor structure, and second transverse leads of said second resistor structure spaced at different distances from said first resistor structure.

10. The method as in claim 9,

wherein said forming a lower semiconductor pattern further includes forming a third resistor structure and a fourth resistor structure, each of said third resistor structure and said fourth resistor structure including a zigzag portion with further transverse leads extending orthogonal to a direction from said third resistor structure to said fourth resistor structure and disposed orthogonal to said transverse leads;

further comprising measuring a third resistance of said third resistor structure and measuring a fourth resistance of said fourth resistor structure; and

wherein said calculating overlay accuracy is further based on said third resistance and said fourth resistance and includes calculating alignment accuracy in the orthogonal directions.

11. The method as in claim 10, wherein said forming a lower semiconductor pattern includes forming a group of said first resistor structure, said second resistor structure, said third resistor structure and said fourth resistor structure on multiple locations of a semiconductor substrate.

12. The method as in claim 11, wherein said transverse leads include first transverse leads of said first resistor structure spaced at different distances from said second resistor structure, second transverse leads of said second resistor structure spaced at different distances from said first resistor structure, third transverse leads of said third resistor structure spaced at different distances from said fourth resistor struc-

ture, and fourth transverse leads of said fourth resistor structure spaced at different distances from said third resistor structure.

13. A method for determining overlay accuracy in a semiconductor device, said method comprising:

forming a lower semiconductor pattern of a silicon material bounded laterally by a dielectric, said lower semiconductor pattern including at least a resistor structure;

forming a first overlying pattern in a first material layer or layers, over said semiconductor pattern;

forming a second overlying pattern in a second material layer or layers, over said semiconductor pattern;

siliciding exposed portions of said lower semiconductor pattern not covered by said first overlying pattern or said second overlying pattern;

measuring a resistance of only said resistor structure, said resistor structure electrically isolated from said first and second overlying patterns; and

calculating alignment accuracy between said first overlying pattern and said second overlying pattern based on said resistance,

wherein said exposed portions comprise a gap between boundaries of said first overlying pattern and said second overlying pattern.

14. The method as in claim 13, wherein said lower semiconductor pattern includes a plurality of parallel leads of different lengths and orthogonal leads coupling ends of each said parallel lead to an adjacent one of said parallel leads.

15. A method for determining overlay accuracy in a semiconductor device, said method comprising:

forming a lower semiconductor pattern of a semiconductor material bounded by a dielectric, said lower semiconductor pattern including a first resistor structure and a second resistor structure;

forming an overlying pattern in a material layer or layers, over said lower semiconductor pattern;

siliciding exposed portions of said first resistor structure and said second resistor structure not covered by said overlying pattern;

measuring a first resistance of said first resistor structure and measuring a second resistance of said second resistor structure; and

calculating overlay accuracy between said overlying pattern and said lower semiconductor pattern based on said first resistance and said second resistance, wherein each of said first resistor structure and said second resistor structure comprises a zig-zag portion including transverse leads disposed orthogonal to a direction from said first resistor structure to said second resistor structure.

16. The method as in claim 1, wherein said lower semiconductor pattern includes each of said first and second resistor structures having a plurality of parallel leads having different lengths and coupled to one another by orthogonal leads and said calculating includes establishing a correlation between a number of said orthogonal leads that were silicided during said siliciding and said first and second resistances.

17. A method for determining overlay accuracy in a semiconductor device, said method comprising:

forming a first pattern of a silicon material on a first device level;

siliciding all portions of said first pattern not covered by at least a further pattern formed at further device levels and electrically isolated from, and not directly contacting, said first pattern;

determining a measured resistance by measuring resistance of only said first pattern after said siliciding; and

establishing a correlation between said measured resistance and overlay accuracy of said at least a further pattern,

wherein said at least a further pattern comprises a duality of further patterns formed of different material layers in two different device levels.

18. The method as in claim **17**, wherein said overlay accuracy is an overlay accuracy between said duality of further patterns.

19. The method as in claim **17**, wherein said overlay accuracy is an overlay accuracy between said at least a further pattern and said first pattern.

20. The method as in claim **13**, wherein said first overlying pattern and said second overlying pattern are each formed of materials that include a lower dielectric layer such that said lower semiconductor pattern first pattern is not electrically connected to first overlying pattern and said second overlying pattern.

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